CLAIMS

1. Method for fabricating an electronic component with self-aligned source, drain and gate, comprising the following steps:

a) the formation of a dummy gate (112) on a silicon substrate (100), said dummy gate defining a position for a channel (121) of the component,

b) at least one implantation of doping impurities in the substrate, to form a source (118) and a drain (120) either side of the channel, using the dummy gate as implanting mask,

c) superficial, self-aligned siliciding of the source and drain,

d) depositing at least one layer of so-called contact metal (130, 132) having a total thickness greater than the height of the dummy gate, and polishing the metal layer stopping at the dummy gate,

e) replacing the dummy gate by at least one final gate (150, 160, 164) separated from the substrate by a gate insulating layer (148), and electrically insulated from the source and drain.

2. Method according to claim 1, in which step d) comprises the depositing of a first metal layer (130) and, above the first layer, a second metal layer (132) having greater mechanical resistance to polishing than the first layer, the thickness of the first metal layer being less than the height of the dummy gate, but the total thickness of the first and second layers being greater than the height of the dummy gate.

3. Method according to claim 1 also comprising, before siliciding, the formation of side spacers (114, 116) on the sides of the dummy gate.

4. Method according to claim 3, in which dual-layer spacers are formed comprising an attachment layer (114) in silicon oxide, in contact with the dummy gate, and a superficial layer (116) in silicon nitride.

5. Method according to claim 2, in which the first metal is chosen from among tungsten and titanium, and in which the second metal is chosen from among TaN, Ta and TiN.

6. Method according to claim 1 comprising, after polishing, superficial oxidation of the metal layer or layers.

7. Method according to claim 1, in which a solid substrate is used.

8. Method according to claim 1, in which a substrate of silicon on insulator type is used.

9. Method according to claim 1, in which step e) comprises the removal of the dummy gate, formation of the gate insulating layer (148), depositing at least one metal layer (150, 160, 162), so-called gate layer, having an overall thickness equal to or greater than the height of the removed dummy gate, and forming said metal layer.

10. Method according to claim 9 comprising, after the formation of the gate insulating layer (148), the depositing of a first gate metal layer (160), the depositing of at least one inter-gate dielectric layer (162), and the depositing of a second gate metal layer (164).